IN THE SPECIFICATION

Please amend the paragraphs of the specification as follows:

Please replace paragraph [0006] with the following amended paragraph:

[0006] The various channels within a given "forward" (base station to mobile unit) TIA/EIA-95 CDMA channel include data channels, a synchronization channel, a pilot channel, and a set of paging channels, all transmitted from the base station to mobile units. The pilot channel carries a reference signal, commonly known as the pilot signal. The pilot signal is a regularly repeated digital pattern of "chips," wherein each chip[[s]] is represented by a single binary digit. In the exemplary embodiment, the pilot signal is a pattern that is 32,768 "chips" in length, which repeats at a chip rate of 1.2288 MHz. Thus, the pattern repeats itself every 26.6 milliseconds (ms).

Please replace paragraph [0010] with the following amended paragraph:

[0010] ~~Figure~~ FIG. 1 is a block diagram of an earlier signal detection circuit or "searcher" 10 that can be used in a mobile unit to check the power of pilot signals at certain given phase offsets or to search for received pilot signals over an entire sequence of phase offsets. Searcher 10 includes a despreader 12, a correlator 14, an energy storage and sorting module 16, and a processing control 18.

Please replace paragraph [0013] with the following amended paragraph:

[0013] ~~Figure~~ FIG. 2 is a schematic diagram of a greatly simplified correlator 14. A detected signal is input into a comparator 112 at input 114 and an expected signal is input into comparator 112 at input 116. For purposes of the present application, it is convenient to discuss the signal transmitted by a base station as a digital signal composed of 1's and -1's. The comparator 112 can perform, for example, a multiplying function such that if the digital components of the signals at inputs 114 and 116 match (e.g. 1,1 or -1,-1), the output 118 is 1, or high, and if the digital components of the signals at inputs

114 and 116 do not match (e.g. -1,1 or 1,-1) the output 118 of comparator 112 is -1, or low.

Please replace paragraph [0026] with the following amended paragraph:

[0026] Prior art ~~Figure~~ FIG. 1 is a block diagram of an earlier pilot signal searcher for use in a digital cellular mobile unit.

Please replace paragraph [0027] with the following amended paragraph:

[0027] Prior art ~~Figure~~FIG. 2 is a block diagram of a greatly simplified correlator for use with the pilot signal searcher shown in ~~Figure~~FIG. 1.

Please replace paragraph [0028] with the following amended paragraph:

[0028] ~~Figure 3a~~FIG 3A is a diagram illustrating a first phase pilot signal and matching detection device detecting of a portion of the first phase pilot signal, and the output of such a matching detection device, in accordance with the present invention.

Please replace paragraph [0029] with the following amended paragraph:

[0029] ~~Figure3b~~ FIG. 3B is a diagram illustrating a second phase pilot signal the matching detection device shown in Figure 3a prior to detecting a portion of the second phase pilot signal, and the commensurate output of the matching detection device, in accordance with the present invention.

Please replace paragraph [0030] with the following amended paragraph:

[0030] ~~Figure 3c~~ FIG. 3C is a diagram illustrating the second phase pilot signal shown in ~~Figure 3b~~FIG. 3B and the matching detection device shown in ~~Figure 3a~~FIG. 3A detecting a portion of the second phase pilot signal, and the commensurate output of the matching detection device, in accordance with the present invention.

Please replace paragraph [0031] with the following amended paragraph:

[0031] ~~Figure 3d~~FIG. 3D is a diagram of a relatively lower power pilot signal and the matching detector shown in ~~Figure 3a~~FIG. 3A detecting the relatively low power pilot signal, and the commensurate output of the matching detection device, in accordance with the present invention.

Please replace paragraph [0032] with the following amended paragraph:

[0032] ~~Figure 4~~FIG. 4 is a block diagram of a pilot signal searcher including a despreading matched filter in accordance with the present invention.

Please replace paragraph [0033] with the following amended paragraph:

[0033] ~~Figure 5~~FIG. 5 is a schematic diagram of a despreading matched filter in accordance with the present invention and which can be used in conjunction with the pilot signal searcher shown in Figure 3.

Please replace paragraph [0034] with the following amended paragraph:

[0034] ~~Figure 6~~ FIG. 6 is a block diagram of the primary searcher shown in ~~Figure 3~~ FIG. 3 which can be used in parallel with the despreading matched filter shown in ~~Figure 5~~ FIG. 5.

Please replace paragraph [0035] with the following amended paragraph:

[0035] ~~Figure 7~~ FIG. 7 is a schematic diagram of a despreading correlator that can be used in conjunction with the primary searcher shown in ~~Figure 5~~ FIG. 5.

Please replace paragraph [0037] with the following amended paragraph:

[0037] ~~Figures 3a, 3b, 3c and 3d~~FIGS. 3A, 3B, 3C and 3D are diagrams illustrating detection of pilot signals in accordance with the present invention. In ~~Figure 3a~~ FIG. 3A, a pilot signal 310 has a specific digital signal pattern of chip values, represented by 1s and -1s. As discussed in the Background section, every pilot signal transmitted by every base station has the same digital signal pattern. However, as indicated above, each pilot signal

may be a shifted version of one another. The pilot signal 310 is received in a serial manner by a mobile unit (not shown). The mobile unit includes a matching detector 312 that is configured with at least a portion of the digital signal pattern of the pilot signal. Specifically, for purposes of illustration, in ~~Figure 3a-3d~~ FIGS. 3A-3D, matching detector 312 is configured with the six chip sequence (1,1,1,-1,-1,1). As discussed below, an actual matching detector is preferably configured with a significantly longer chip sequence. The matching detector can be either programmed into software or, as discussed below, can be a hardware circuit.

Please replace paragraph [0038] with the following amended paragraph:

[0038] When the mobile unit receives a pilot signal 310, it actually receives a mixture of the transmitted signal and noise. For the purposes of simplicity, the received mixture of pilot signal 310 and noise is hereinafter referred to as pilot signal 310. As pilot signal 310 is serially received by the mobile unit, a portion of digital signal pattern of the pilot signal 310 is compared to the digital signal pattern configured in the matching detector 312. Because the matching detector 312 is configured with at least a portion of the specific digital pilot signal pattern, at some point during the serial receipt of the pilot signal 310, the portion of the pattern of the pilot signal 310 that is being compared will likely match the pattern configured in the matching detector 312. This situation is shown in ~~Figure 3a~~ FIG 3A. Specifically, the portion 314 of the pilot signal 310 matches the portion of the pilot signal pattern configured in matching detector 312. When the match occurs, the matching detector can generate a match signal.

Please replace paragraph [0039] with the following amended paragraph:

[0039] Although ~~Figure 3a~~FIG 3A shows a complete match between matching detector 312 and portion 314 of pilot signal 310, due primarily to noise in a received pilot signal, a complete match of all the chips of the portion of the pilot signal pattern that is configured in the matched detector may not occur. Thus, preferably, the matching detector can be configured to generate a different magnitude signal depending upon the number of chips that match. Preferably, though not necessarily, the greater the number of chips that

match, the greater the magnitude of the signal generated by the matching detector 312. Thus, as shown in ~~Figure 3a~~ FIG. 3A, the signal 316 generated by the matching detector 312 can, for example, be a voltage, and the more chips that match, the higher the voltage signal generated. Accordingly, on a relatively complete match, the matching detector 312 would generate a relatively high voltage spike 316, as shown on grid 315 in ~~Figure 3a~~ FIG. 3A, at the point in time during which the relatively complete match occurs. Indicating time on horizontal axis 350, the relative time is indicated as t1. The magnitude of the voltage spike, indicating a match, and the relative time at which the spike occurred, t1, can then be stored in a local memory.

Please replace paragraph [0040] with the following amended paragraph:

[0040] As discussed in the background section, the digital chip pattern is the same for a pilot signal transmitted by any base station. However, the phase of the pilot signals transmitted by different base stations is shifted. ~~Figure 3b~~ FIG. 3B shows a second pilot signal 320 having the same digital pattern of +1s and -1s as first pilot signal 310, but shifted in phase by time t2. This can be seen by the fact that the portion 324 of pilot signal 320 that matches the chips configured in matching detector 312 is shifted from the identical portion 314, in pilot signal 310, by time t2. Thus, no match will occur between matching detector 312 and second pilot signal 320 at relative time t1. Therefore, the signal 326 output by matching detector 312, shown on time vs. voltage grid 325, will have a relatively small magnitude at relative time t1.

Please replace paragraph [0041] with the following amended paragraph:

[0041] However, as shown in ~~Figure 3c~~ FIG. 3C, at relative time t3, which is offset from time t1 by the phase shift time of t2, matching detector 312 will indicate a match of the pilot signal 320. Thus, as shown on time vs. voltage grid 335, the signal 336 output by matching detector 312 will be relatively large at time t3. As with pilot signal 310, the magnitude of signal 336, indicating a match, and the relative time at which the match occurred, t3, can be stored in a local memory.

Please replace paragraph [0044] with the following amended paragraph:

[0044] This situation is shown in ~~Figure 3d~~ FIG. 3D, which shows a third pilot signal 330 that is weaker than first pilot signal 310. Box 334 shows the portion of the digital chip pattern of pilot signal 330 that is configured in matching detector 312. This portion of pilot signal 330 should match with the chips configured in matching detector 312 at time t1. However, as shown, because of errors due to noise, fewer than all of the chips configured in the matching detector 312 are matched in the portion 334 of pilot signal 330. Specifically, the third and fourth chips in portion 314 have been inverted, by noise arriving with the signal, from a 1 to a -1 and from a -1 to a 1, respectively. Thus, as shown in time vs. voltage grid 345, the magnitude of the signal 346 generated by matching detector 312 is relatively lower than the magnitude of the signal 316 generated by more powerful pilot signal 310. This indicates that while the mobile unit is receiving a pilot signal 330, it is weaker than pilot signal 310, and, therefore, probably less appropriate for synchronization.

Please replace paragraph [0047] with the following amended paragraph:

[0047] It is also within the ambit of the present invention to use a matching detector as described above in parallel with the type of correlator shown in ~~Figure 2~~FIG. 2 and described in the Background section. As discussed in the Background section, the correlator can search at a first phase offset and then, if no significant energy is being detected, switch to searching at any other phase offset, which may be hundreds or thousands of chips from the first phase offset, simply by changing the phase of the reference signal. Additionally, while the maximum energy information in a correlator would be obtained by a full 26.6 ms search, if no significant or unexpected energy is being detected at a given phase offset after only a portion of 26.6 ms, the search could be abandoned and a new search could be initiated at another phase offset.

Please replace paragraph [0051] with the following amended paragraph:

[0051] ~~Figure 4~~FIG. 4 is a block diagram showing an embodiment of a matched filter assisted signal detection circuit or searcher 210 in accordance with the present invention. Searcher 210 includes a despreading matched filter 212, the output of which is fed into energy storage and sorting module 214. Energy storage and sorting module 214 is connected to a processing control 218. Searcher 210 also includes a primary searcher 216 in parallel to the despreading matched filter 212. Primary searcher 216 can be similar to the prior art searcher 10 discussed above. Primary searcher 216 is also connected to processing control 218.

Please replace paragraph [0052] with the following amended paragraph:

[0052] Despreading matched filter 212 is for despreading and detecting pilot signals received by a mobile unit in which searcher 210 is deployed. ~~Figure 5~~ **FIG. 5** is a schematic diagram showing one embodiment of despreading matched filter 212. As discussed in the Background section, a PN pilot signal includes both an in-phase (I) and quadrature (Q) component. To accommodate these two signal components, matched filter 212 includes an I-input 220 and a Q-input 222. Matched filter 212 also includes a plurality of I-taps ~~224a, 224b, 224c, and 224d~~224A, 224B, 224C, and 224D for holding and reading values of a single pilot signal pattern component (e.g., a single bit or chip). I-Taps ~~224a-224d~~ 224A-224D are distributed sequentially along an I-primary line 228. A Q-primary line 230 includes a plurality of Q-taps ~~225a, 225b, 225c and 225d~~ 225A, 225B, 225C and 225D distributed sequentially there-along. Between each adjacent pair of taps ~~224a-224d and 225a-225d~~224A-224D and 225A-225D, is a delay circuit 226 for holding a chip value on each tap for a predetermined amount of time. Delay circuits 226 can be any devices that will delay transmission of a signal from the input to the output for a predetermined period of time and are preferably simple latches.

Please replace paragraph [0053] with the following amended paragraph:

[0053] Preferably, at the end of the I-primary line 228, adjacent to an I-output 233, is an I-integrator 234 and at the end of the Q-primary line 230, adjacent to a Q-output 235, is a

Q-integrator 236. The I-integrator 234 and Q-integrator 236 are for summing chip values held on the taps ~~224a-224d and 225a-225d~~224A-224D and 225A-225D. A plurality of tap lines 240a - 240h connect the I-taps ~~224a-224d~~224A-224D and Q-taps ~~224a-225d~~224A-225D to the I-integrator 234 and Q-integrator 236. The I-output 233 and Q-output 235 are then fed into a final integrator 239. Final integrator 239, in the exemplary embodiment, sums the squares of I-output 233 and Q-output 235, and produces a matched filter voltage output, matched filter output 242, accordingly. Matched filter output 242 feeds into energy storage and sorting module 214._Matched filter 212 detects a pilot signal that matches a predetermined digital pattern by outputting a relatively large energy signal when a match is detected. Additionally, it despreads the pilot signal that was initially spread by the base station, as discussed in the background section. This despreading is implemented to compensate for any relative shift in phase that may have occurred to the pilot signal in transmission of the signal from the base station. Preferably, matched filter 212 implements a QPSK despreading scheme. However, it is within the scope of the present invention for matched filter 212 to implement any type of despreading scheme.

Please replace paragraph [0054] with the following amended paragraph:

[0054] To perform these functions, the I-component of a received digital pilot signal is fed into the I-input 220 and the Q-component of the received pilot signal is fed into the Q-input 222. The rate at which the Q- and I-components of the pilot signal are fed into the inputs 220 and 222, respectively, that is, the "sampling" rate of matched filter 212, allows one chip of the pilot signal to be placed on the taps ~~224a and 225a~~224A and 225A, respectively, per sample. This sampling rate is preferably simply the frequency of the pilot signal, which in the present embodiment is 1.2288 MHz. The first delay circuits 226 in the I-primary line 228 and Q-primary line 230 then delay the pilot signal, preferably holding the chip values on the first taps ~~224a and 225a~~224A and 225A for approximately .81 microseconds, the period of a pilot chip. The delays 226 then pass the chip values on taps ~~224a and 225a~~224A and 225A to taps ~~224b and 225b~~224B and 225B, respectively.

Please replace paragraph [0055] with the following amended paragraph:

[0055] Because in a presently preferred embodiment, .81 microseconds is the period of a pilot chip, this delay time allows a second chip value of the pilot signal to be placed on the taps ~~224a and 225a~~ 224A and 225A simultaneously with the transfer from taps ~~224a and 225a~~ 224A and 225A to taps ~~224b and 225b~~ 224B and 225B, respectively, of the first chip value. This process continues until each tap ~~224a 224d and 225a 225d~~ 224A-224D and 225A-225D in matched filter 212 has a chip value.

Please replace paragraph [0056] with the following amended paragraph:

[0056] Each time a sample is taken, that is, preferably approximately every .81 microseconds, the chip values at the nth tap are routed to the I- and Q-integrators 234 and 236, respectively, via tap lines ~~240a 240h~~ 240A-240H, according to chart 1 below.

$I\text{-expected}_n$	$Q\text{-expected}_n$	$I\text{-out}_n$	$Q\text{-out}_n$
1	1	I_n	Q_n
1	-1	$-Q_n$	I_n
-1	1	Q_n	$-I_n$
-1	-1	$-I_n$	$-Q_n$

Chart 1

Please replace paragraph [0057] with the following amended paragraph:

[0057] By routing the I-and Q-component chip values to the I- and Q-integrators as in Chart 1, the matched filter 212 both despreads the input QPSK pilot signal and provides a maximum output when a predetermined signal is matched. The predetermined sequence of chip values for which the matched filter searches is configured into the matched filter by the interconnection or mapping of tap lines ~~240a 240h~~ 240A-240H with I- and Q-integrators 234 and 236, respectively, an example of which is shown in Figure 5. In the manner explained below, Chart 1 can be used as a "key" to determine how to interconnect tap lines ~~250a 240h~~ 250A-240H with I- and Q-integrators 234 and 236 respectively to

QPSK despread the input pilot signal and provide a maximum output when a predetermined signal is matched.

Please replace paragraph [0058] with the following amended paragraph:

[0058] To detect the predetermined pilot sequence having an I-chip sequence of, for example, 1,-1,-1,1 and Q-chip sequence of, for example, -1,-1,1,1, according to a QPSK despreading scheme, the tap line interconnection or mapping shown in ~~Figure 5~~ FIG. 5 would be implemented. This mapping is completed according to Chart 1. The first and second columns of chart 1, labeled (I-expected$_n$, Q-expected$_n$), respectively, show each of the four I- and Q-chip value combinations that could possibly make up a single set of simultaneous I- and Q-chip values of a predetermined pilot sequence, that is, the four possible values for the pair (I-expected$_n$, Q-expected$_n$). Specifically, (1,1) in the first row, (1, -1) in the second row, (-1,1) in the third row, and (-1,-1) in the fourth row. The third and fourth columns of chart 1 show how the actual value on an I-tap (In) and Q-tap (Qn) are routed to the I-integrator 234 (I-outn) or Q-integrator 236 (Q-outn) in order to both QPSK despread the pilot signal and to provide a maximum output of matched filter 212 when the predetermined pilot signal is received.

Please replace paragraph [0059] with the following amended paragraph:

[0059] For example, the first row of Chart 1 shows how to connect an I-tap and Q-tap to the I-integrator 234 and Q-integrator 236 if the expected chip value on the I-tap will be 1 simultaneous with an expected chip value of 1 on the Q-tap, that is, for an (I-expected[[n]]$_n$, Q-expected[[n]]$_n$) combination of (1,1). The "In" in the I-outn column (the third column) of the first row indicates that, for an (I-expected[[n]]$_n$, Q-expected[[n]]$_n$)=(1,1), the actual value on the I-tap is directly routed to, that is, directly wired to, the I-integrator 234. The "Qn" in the Q-outn column (the fourth column) of Chart 1 indicates that for an (I-expected[[n]]$_n$, Q-expected[[n]]$_n$)=(1,1) the actual value on the Q-tap is directly routed to, that, directly wired to, the Q-integrator 234.

Please replace paragraph [0060] with the following amended paragraph:

[0060] For a predetermined pilot sequence having an I-chip sequence of, 1,-1,-1,1 and Q-chip sequence of, -1,-1,1,1, the I-tap and Q-tap that would be interconnected to integrators 234 and 236 to produce a maximum output for an (I-expected[[n]]$_n$, Q-expected[[n]]$_n$)=(1,1) would be taps ~~224d and 225d~~ 224d and 225d. This is because in the expected pilot sequence, the (I-expected[[n]]$_n$, Q-expected[[n]]$_n$) of (1,1) is the fourth combination to occur in the predetermined pilot sequence, and I-tap [[224d]] 224D and Q-tap [[225d]] 225D are the pair of taps that are fourth along the I-primary line 228 and Q-primary line 230, respectively, from the I-input 220 and Q-input 222, respectively.

Please replace paragraph [0061] with the following amended paragraph:

[0061] Thus, as shown in ~~Figure 5~~ FIG. 5, the I-tap value, 1, is directly routed to the I-integrator 234 via tap line 240d and the Q-tap value, 1, is directly routed to the Q-integrator 236 via tap line 240h. This provides the maximum values, 1 and 1, to I- and Q-integrators 234 and 236, respectively, to generate a maximal output value.

Please replace paragraph [0062] with the following amended paragraph:

[0062] The second row of Chart 1 shows how an I-tap and Q-tap would be interconnected to integrators 234 and 236 for an (I-expected[[n]]$_n$, Q-expected[[n]]$_n$) = (1,-1). To generate a maximum matched filter output signal, and QPSK despread the input pilot signal, for (I-expectedn, Q-expectedn)=(1,-1) the "-Qn" in the I-outn column of the second row indicates that the actual value on the Q tap be inverted and routed to the I-integrator 234. The "In" in the Q-outn column of the second row indicates that the actual value on the I-tap be directly routed to the Q-integrator 236. For the example, predetermined pilot sequence having an I-chip sequence of, 1,-1,-1,1 and Q-chip sequence of, -1,-1,1,1, the (I-expected[[n]]$_n$, Q-expected[[n]]$_n$) of (1,-1) occurs as the first combination. Thus, I-tap and Q-tap that would be interconnected to integrators 234 and 236 to produce and maximum output for an (I-expected[[n]]$_n$, Q-expected[[n]]$_n$)=(1,-1) would be I-tap [[224d]] 224D and Q-tap [[225d]] 225D, the first pair of taps in the primary lines 228 and 230 after inputs 220 and 222.

Please replace paragraph [0063] with the following amended paragraph:

[0063] Thus, as shown in ~~Figure 5~~ FIG. 5, the I-tap value, 1, on I-tap [[224a]] 224A is routed to the Q-integrator 236 via tap line [[240a]] 240A and the Q-tap value, -1, on Q-tap [[225a]] 225A is routed via tap line [[240e]] 240E through an inverter [[241e]] 241E, to the I-integrator 236. Thus, when the input chip value matches the expected chip value, a 1 is routed to both integrators 234 and 236 to maximize the sum for taps ~~224a and 225a~~ 224A and 225A.

Please replace paragraph [0064] with the following amended paragraph:

[0064] The third and fourth rows of Chart 1 are implemented in the manner described above with respect to the first and second rows of Chart 1. In the third row, for (I-expectedn, Q-expectedn) = (-1,1), as is the case on taps ~~224c and 225c~~224C and 225C, the I-tap value, -1, is routed via tap line [[240c]] 240C through inverter [[241c]] 241C, to the Q-integrator 236 and the Q-tap value, 1, is routed via tap line [[240g]] 240G directly to the I-integrator 234. Because the I value, -1, is inverted, and the Q value, 1, is routed directly, the integrators 234 and 236 add maximally to the sum for taps ~~224c and 225c~~224C and 225C when there is a match on taps ~~224c and 225c~~224C and 225C to the expected values of (-1,1). Finally, if (I-expectedn, Q-expectedn) = (-1,-1), as it would on taps ~~224b and 225b~~, 224B and 225B the I-tap value, -1, is routed through inverter [[241b]] 241B to the I-integrator 234 via tap line [[240b]] 240B and the Q-tap value, -1, is routed through inverter [[241f]] 241B to the Q-integrator 236 via tap line [[240f]] 240F. Again, this mapping generates a maximal sum in integrators 234 and 236 for taps ~~224d and 225d~~ 224D and 225D when there is a match on these taps to the expected value of (1,1).

Please replace paragraph [0065] with the following amended paragraph:

[0065] Each integrator 234 and 236 sums the inputs from the tap lines ~~240a-240h~~240A-240H. The I-output 233 and Q-output 235 are then fed into a final integrator 239. Final integrator 239 preferably squares value of the I-output 233 and Q-output 235 signals and preferably sums the result. In this way, the final integrator 239 effectively generates an

energy measurement from the voltage signals. This energy measurement can be a multiple bit digital signal and will be relatively large for times at which the digital signal on the taps of the matched filter match the matched filter's predetermined sequence.

Please replace paragraph [0066] with the following amended paragraph:

[0066] Only eight taps ~~224a-224d and 225a-225d~~224A-224D and 225A-225D are shown in matched filter 212. For a digital signal length of 32,768 chips, up to 32,768 taps in each primary line of the matched filter could be used. However, to manufacture a matched filter with such a large number of taps would be extremely difficult and relatively expensive, and it is unnecessary. In order to detect the presence of the pilot signal pattern, only a portion of the chip pattern need be used. However, to minimize the likelihood of a false match, matched filter 212 preferably has at least 16 taps in each primary line 228, 230. More preferably, matched filter 212 includes approximately 1024 taps; 512 in I-primary line 228 and 512 in Q-primary line 230.

Please replace paragraph [0068] with the following amended paragraph:

[0068] As discussed above, in matched filter 212, 1 values are routed from the taps to the integrators 234 and 236 only when the actual value on a tap matches an expected value. Otherwise, a -1 is routed to the integrators 234 and 236, which reduces the magnitude of the output of the integrators 234 and 236 and reduces the magnitude of the output of matched filter 212 from final integrator 239. Thus, the greater the number of received chip values that match the expected chip values on the taps of matched filter 212, the greater the magnitude of the output of matched filter 212. As explained above with respect to ~~Figures 3a-3D~~FIGS. 3A-3D, the stronger the pilot signal, the greater the number of received chip values of that pilot signal which will match the predetermined pilot sequence. Thus, the magnitude of the output of matched

Please replace paragraph [0071] with the following amended paragraph:

[0071] As shown in ~~Figure 4~~FIG. 4, the output of energy storage and sorting module 214 is fed into processing control 218. Processing control 218 can include a standard

microprocessor, memory elements, and data and address busses. Processing control 218 generally controls the operation of the mobile unit. Additionally, processing control can monitor or control the operation of matched filter 212 and energy storage and sorting module 214 via bus lines 217 and 215, respectively. For example, it could set threshold energy values which energy storage and sorting module 214 is to store or clear stored values out of energy storage and sorting module 214. Implementation and configuration of a microprocessor and other components to perform these functions are described below.

Please replace paragraph [0072] with the following amended paragraph:

[0072] As discussed in the background section, once the mobile unit locates and acquires a relatively strong pilot signal, the pilot signal synchronizes the time base of the mobile unit with the base station that sent the pilot signal. In this way, the mobile unit is provided with the absolute phase offset of the relatively strong pilot signal it is receiving. By comparing when primary searcher 216 detects the pilot of the currently synchronized base station to the times at which matched filter 212 detects each relatively strong pilot signal, processing control 218 can determine the absolute phase offsets of each pilot signal detected by matched filter [[218]] 212.

Please replace paragraph [0076] with the following amended paragraph:

[0076] As shown in ~~Figure 4~~ FIG. 4, matched filter 212 and energy storage and sorting module 214 is preferably used in parallel with primary searcher 216. ~~Figure 6~~ FIG. 6 is a block diagram showing the components of primary searcher 216. Primary searcher 216 is similar to searcher 10 discussed in the Background and includes a despreading correlator 250 and an energy storage and sorting module 252. A schematic illustrating a preferred embodiment of despreading correlator 250 is shown in ~~Figure 7~~FIG. 7. Despreading correlator 250 correlates I- and Q-input signals with an expected, or searched for, I- and Q-input signal, as correlator 14 does with a single expected signal. Correlator 250 also despreads the pilot signal input, preferably using a QPSK scheme, to correct for any relative phase shifts that may have occurred to pilot signal 310 during transmission.

Please replace paragraph [0077] with the following amended paragraph:

[0077] Despreading correlator 250 includes an I-input 262 and a Q-input 260, each of which are connected to a Q-multiplexer (Q-MUX) 264 and an I-multiplexer (I-MUX) 266. The output of Q-MUX 264 is determined by the state of control line 268 and the output of I-MUX 264 is determined by the state of control line 270. The state of control lines 268 and 270 is determined by I-expected$[[n]]_n$ input 272 and Q-expected$[[n]]_n$ input 274 to exclusive-or (XOR) gate 276. I-expected$[[n]]_n$ and Q-expected$[[n]]_n$ are the I- and Q- components, respectively, of the pilot signal for which despreading correlator 250 is searching, that is, the expected pilot signal. Control line 270 contains an inverting buffer 278 to invert the state output by XOR gate 276. The output of Q-MUX 264 serves as one input into XOR gate 278. The other input to XOR gate 278 is I-expected$[[n]]_n$, the I-component of the pilot signal for which primary searcher 216 is searching. The output of I-MUX 266 serves as one input into XOR gate 280. The other input to XOR gate 280 is Q-expected$[[n]]_n$, the Q component of the pilot signal for which primary searcher 216 is searching.

Please replace paragraph [0079] with the following amended paragraph:

[0079] Despreading correlator 250 performs QPSK despreading and correlating on an input signal according to Chart 1 above. Despreading correlator 250 outputs the (In, Qn) required by chart 1 for an expected digital signal input (I-expected$[[n]]_n$, Q-expected$[[n]]_n$). For example, for (I-expected$[[n]]_n$, Q-expected$[[n]]_n$) = (1,-1), according to the second row of Chart 1, the I-outn,[[,]] which is the signal routed to the I-integrator 282, should be -Qn, and the Q-outn,[[,]] which is the signal routed to the Q-integrator, should be In. Thus, if the received Iin and Qin is the expected signal, that is (1,-1), then -Qn = 1 and this value is routed to the I-integrator 282 and In = 1, and this value is routed to the Q-integrator 284.

Please replace paragraph [0080] with the following amended paragraph:

[0080] Despreading correlator performs this function as follows: For (I-expected$[[n]]_n$, Q-expected$[[n]]_n$) = (1,-1), the output of XOR gate 276 is 1. Thus, Q-MUX 264 selects

the value of [[Qin]] Q_{in}, -1, to feed XOR gate 278. If the sampled pilot signal matches this expected signal, that is ~~(Iin, Qin)~~(I_{in}, Q_{in}) = (1,-1), then I-expected$_n$ = 1 and XOR gate 278 outputs a 1 to maximally add to the sum performed by Q-integrator 282. On the I-channel, if the output of XOR 276 is 1, then, due to inverter 278, the control input to I-MUX 266 will have a value of -1. This places [[Iin]]I_{in} on I-MUX output 292. For [[Iin]]I_{in} = 1, and Q-expected = -1, the output of XOR gate 280 will be 1, which maximally adds to the sum performed by I integrator 284. Matching of other possible combinations of (I-expected[[n]]$_n$, Q-expected[[n]]$_n$) listed in Chart 1 similarly result in 1's being summed by integrators 282 and 284. In this way, the signals generated by Q-integrator 282 and I-integrator 284 will be relatively large when the pattern of the input signal ~~(Iin, Qin)~~(I_{in}, Q_{in}) matches the pattern of the expected signal (I-expectedn, Q-expectedn).

Please replace paragraph [0083] with the following amended paragraph:

[0083] Because +1's are routed to integrators 282 and 284 only when there is a match of an expected signal, if the received signal does not precisely match the expected signal, some -1's will be routed to integrators 282 and 284. This reduced the magnitude of the output of these integrators and, therefore, the output of despreading correlator 250 from final integrator 286. As discussed above with respect to ~~Figures 3a-3d~~ FIG. 3A-3D, the stronger the pilot signal being received, the more actual chip values will match the ideal, predetermined pilot sequence chip values. Thus, the stronger the pilot signal being received, the more +1's are summed by integrators 282 and 284, and the fewer -1's that are summed thereby, and the higher magnitude of the output of despreading correlator 250. In this way, the magnitude of the output of despreading correlator provides an indication of the relative strength of a received pilot signal.

Please replace paragraph [0085] with the following amended paragraph:

[0085] The final output 288 of despreading and correlating module 250 is preferably fed into energy storage and sorting module 252. This module can be substantially identical to energy storage and sorting module 214, shown in ~~Figure 4~~ FIG. 4, and can operate in

substantially the same manner. It is also contemplated that both matched filter 212 and despreading correlator 250 feed into the same energy storage and sorting module.